0.18 μm CMOS Fully Differential CTIA for a 32x16 ROIC for 3D Ladar Imaging Systems

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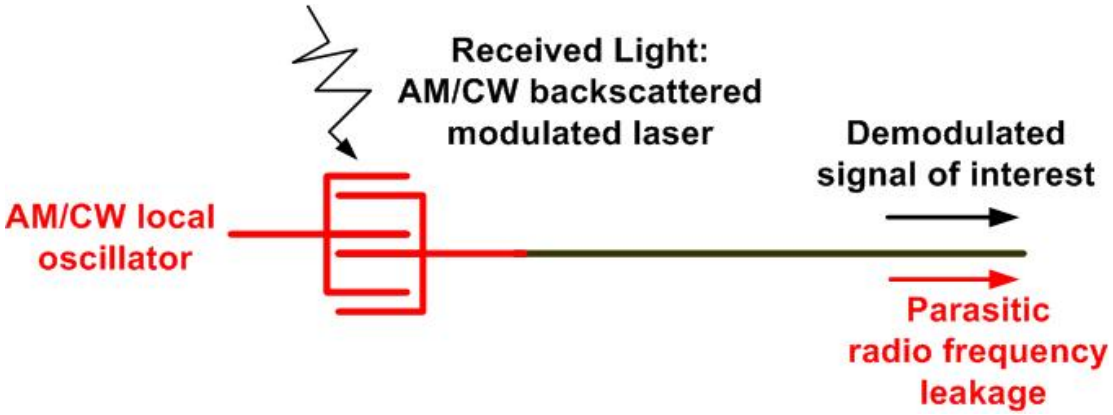
Presentation Outline

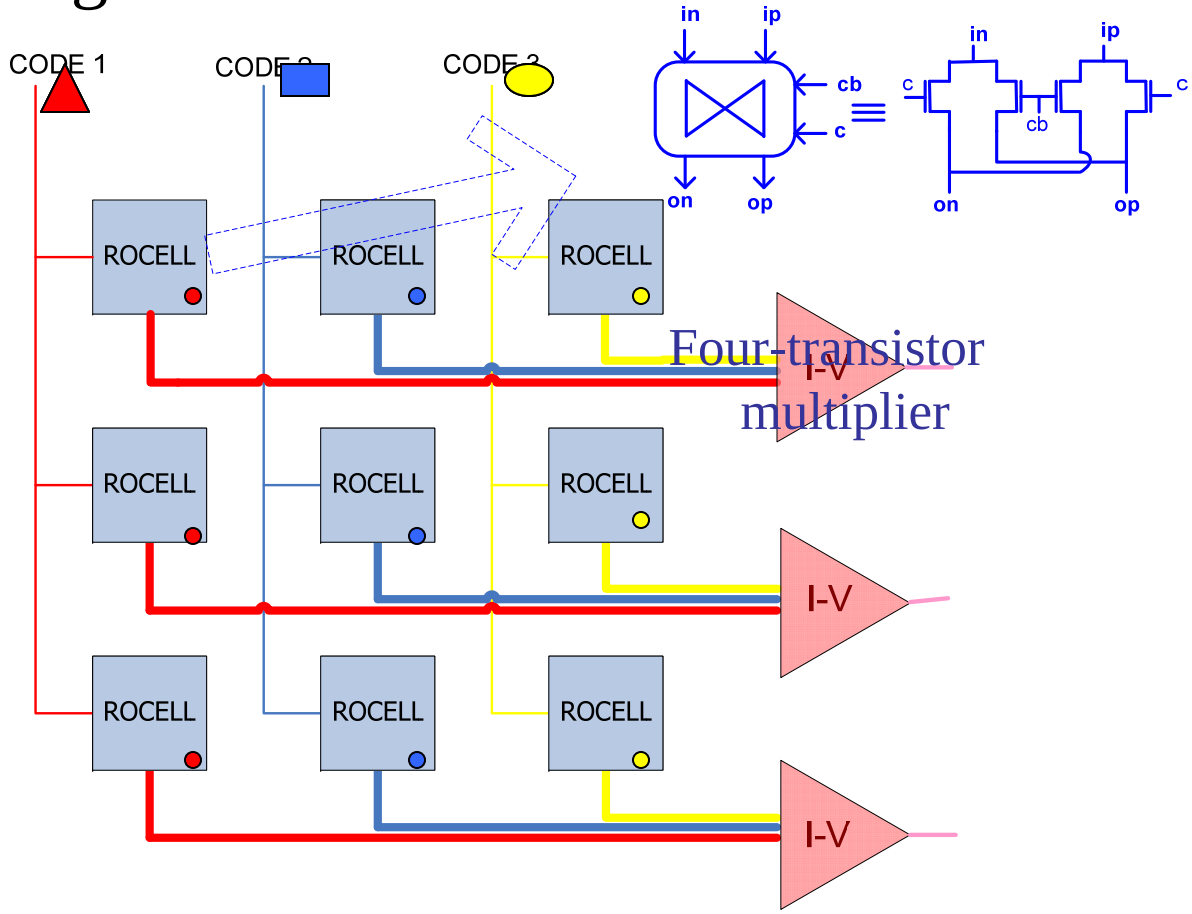
- Introduction
  - Photo-detection for AM/CW LADAR using MSM detectors
  - CDMA ROIC architecture
- Fully Differential Channel
  - Differential MSM photo-detector
  - Differential CDS CTIA
  - Mitigation of RF leakage current
- Design Implementation
  - Floor plan and Layout
  - Post-layout Simulation
- Future work
  - Testing methodology

AM/CW Ladar Photo-detection



- RF modulation and demodulation
- Parasitic leakage current
  - Four to five orders of magnitude > signal of interest

Code Division Multiple Access Readout Integrated Circuit Architecture



- Orthogonal sets of codes
- Column-wise encoding

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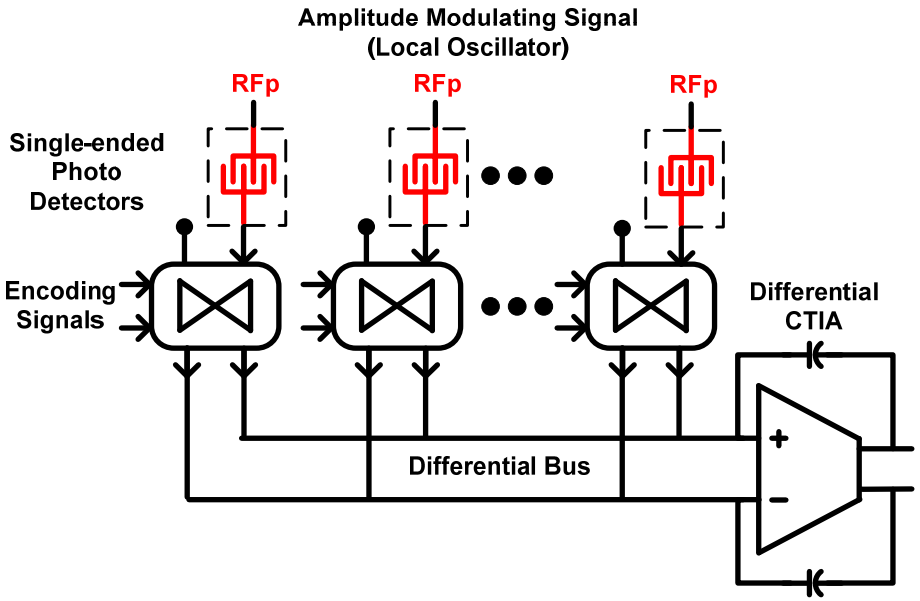
Fully Differential Readout Channel

Single-ended MSM photodetector

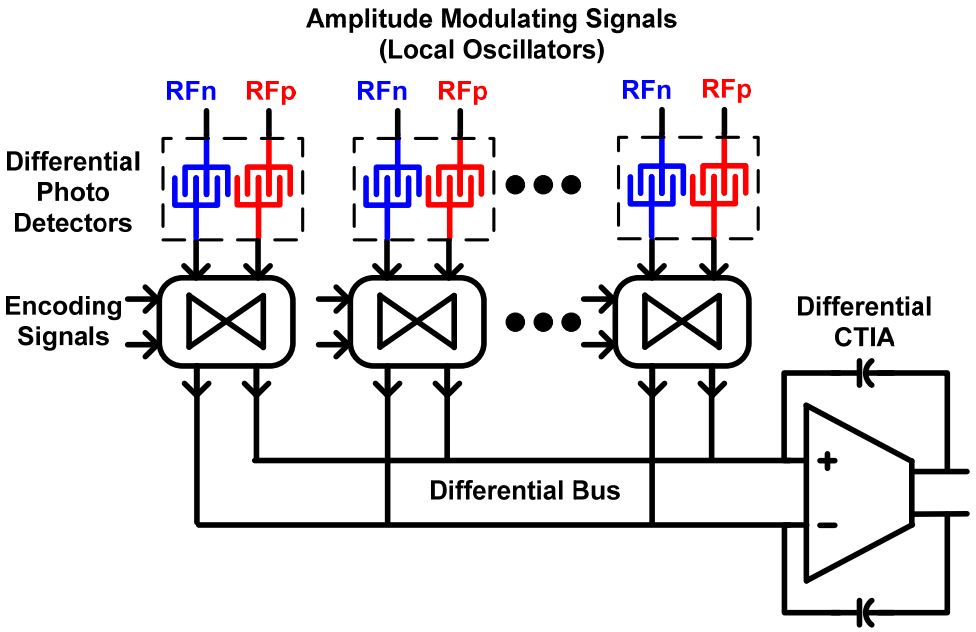
- Disadvantages
  - Not fully Differential architecture
  - Non balanced charged injection in the encoding cell



Fully Differential Readout Channel

Differential MSM photodetector

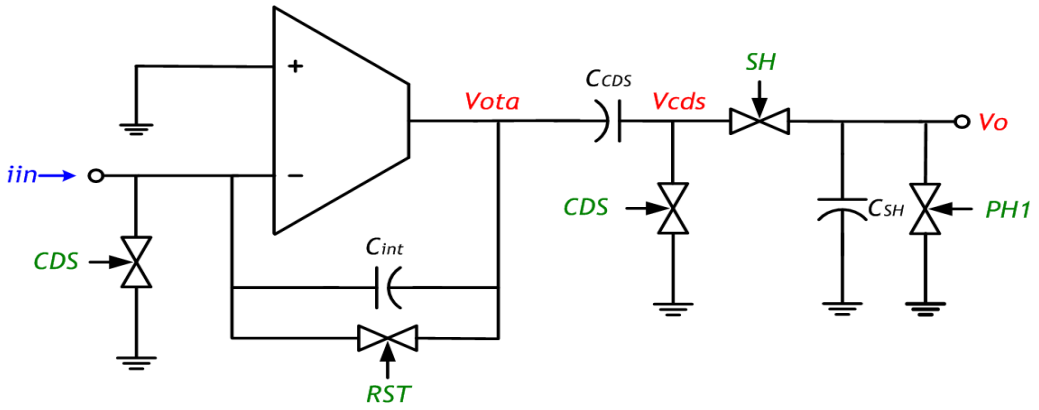
- Advantages
  - Cancel charge injection imbalance
  - Obtain true and complementary output signals at once



Fully Differential Readout Channel

Differential Correlated Double Sampling
Capacitive Trans-impedance Amplifier (1)

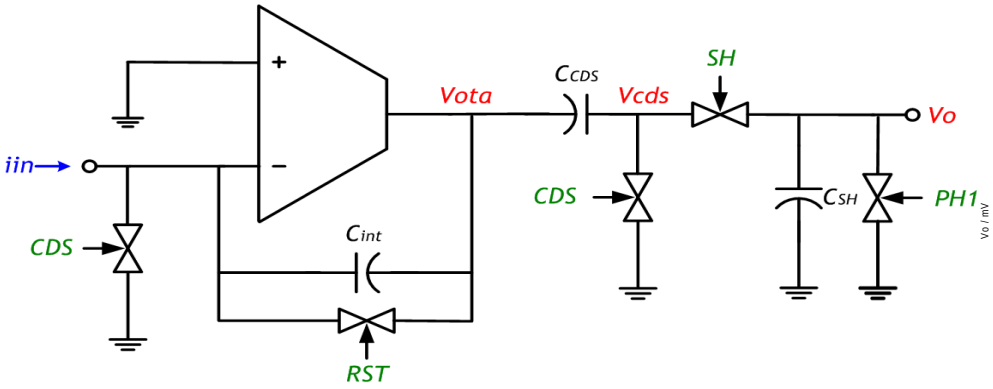
- Things to worry about
  - Thermal noise (RTIA)
  - Sampling noise (CTIA)
- Solution
  - Correlated double sampling (CDS) capacitive trans-impedance amplifier

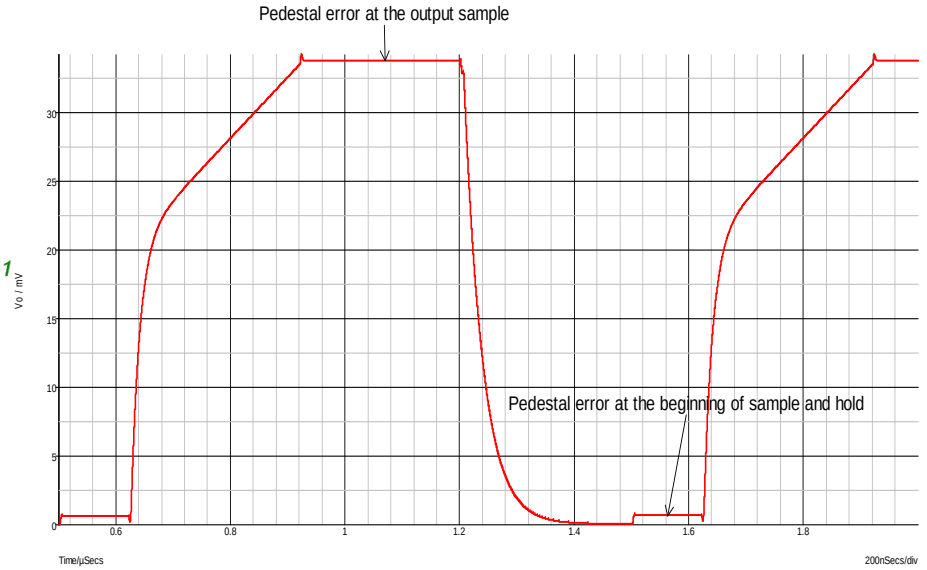


Fully Differential Readout Channel

Differential Correlated Double Sampling
Capacitive Trans-impedance Amplifier (2)

- Single-ended CDS CTIA
  - Charge injection causing pedestal errors

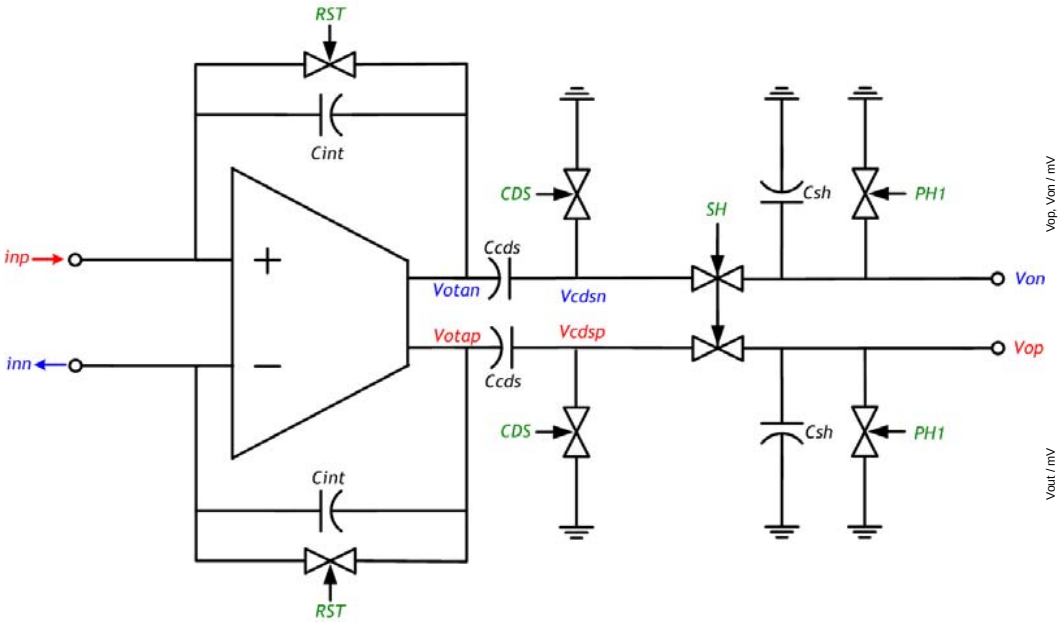


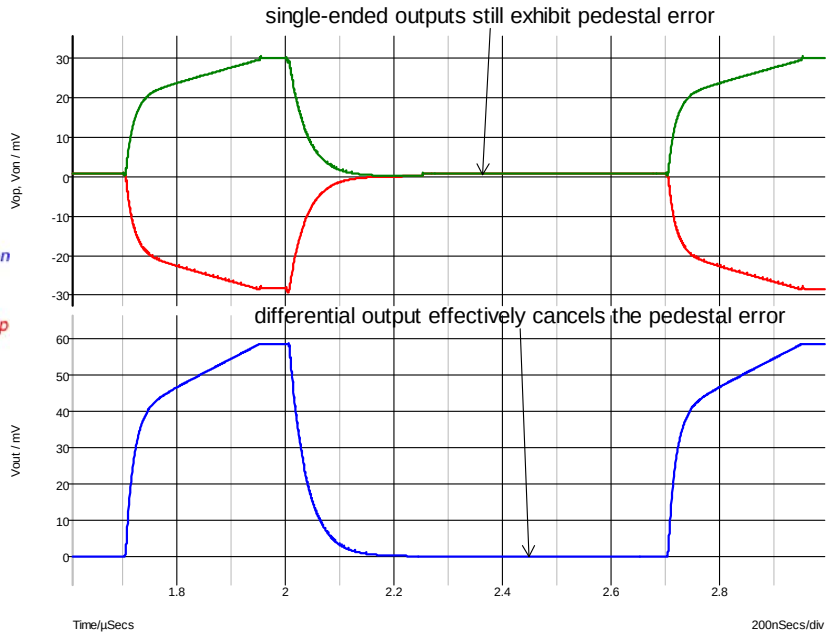


Fully Differential Readout Channel

Differential Correlated Double Sampling
Capacitive Trans-impedance Amplifier (2)

- Differential CDS CTIA
  - Charge injection cancellation
  - True and complementary signal integration



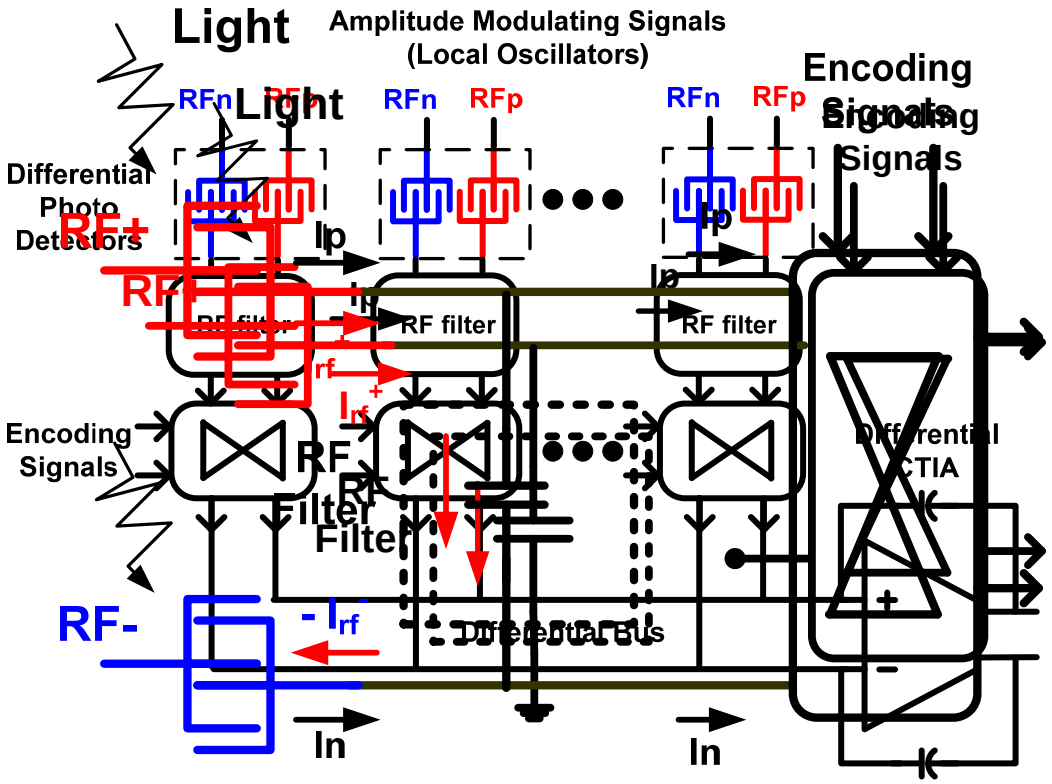


Fully Differential Readout Channel

Mitigation of radio frequency leakage current

- Filter RF before the Encoding cell
  - LC-ladder filters
  - RC-ladder filters
  - Shunt Capacitor

Moreover, Differential Shunt Capacitor



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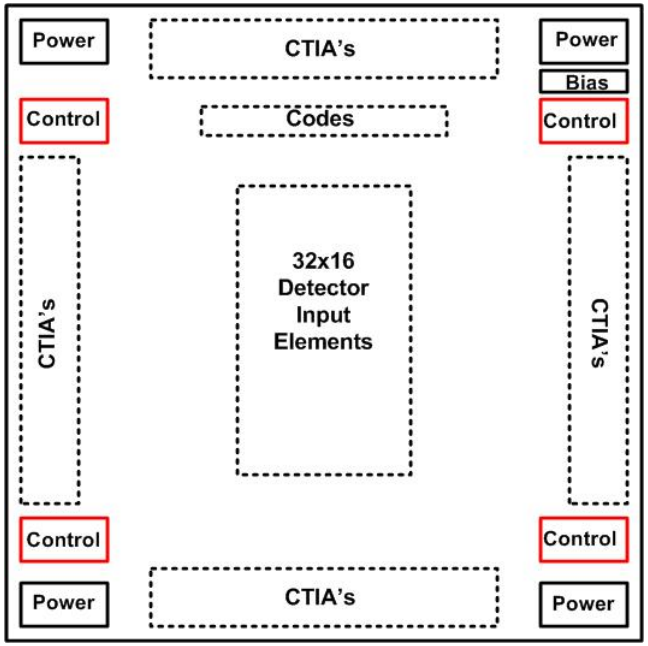
Design Implementation

- 0.18 *μm CMOS 32x16 Fully Differential ROIC*
  - 32x16 MSM Differential detector
  - 32 CDS CTIA's
  - Highly Scalable
    - Special Layout of Components
      - Detector Elements
      - CTIA's



Design Implementation

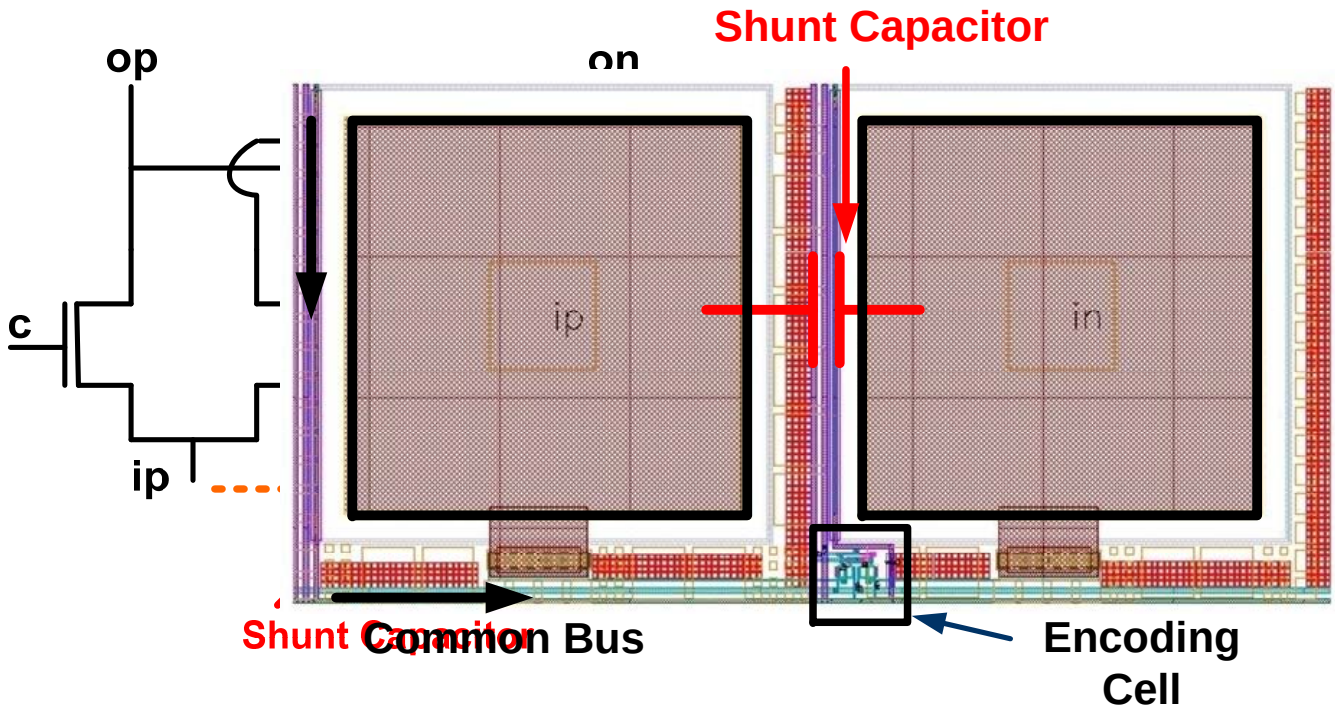
Differential Input Element

- Four transistor encoding cell
- Differential detector bond pad
- Parasitic shunt capacitor

Size

100 μm height

200 μm width



Design Implementation

Differential Correlated Double Sampling
Capacitive Trans-impedance Amplifier

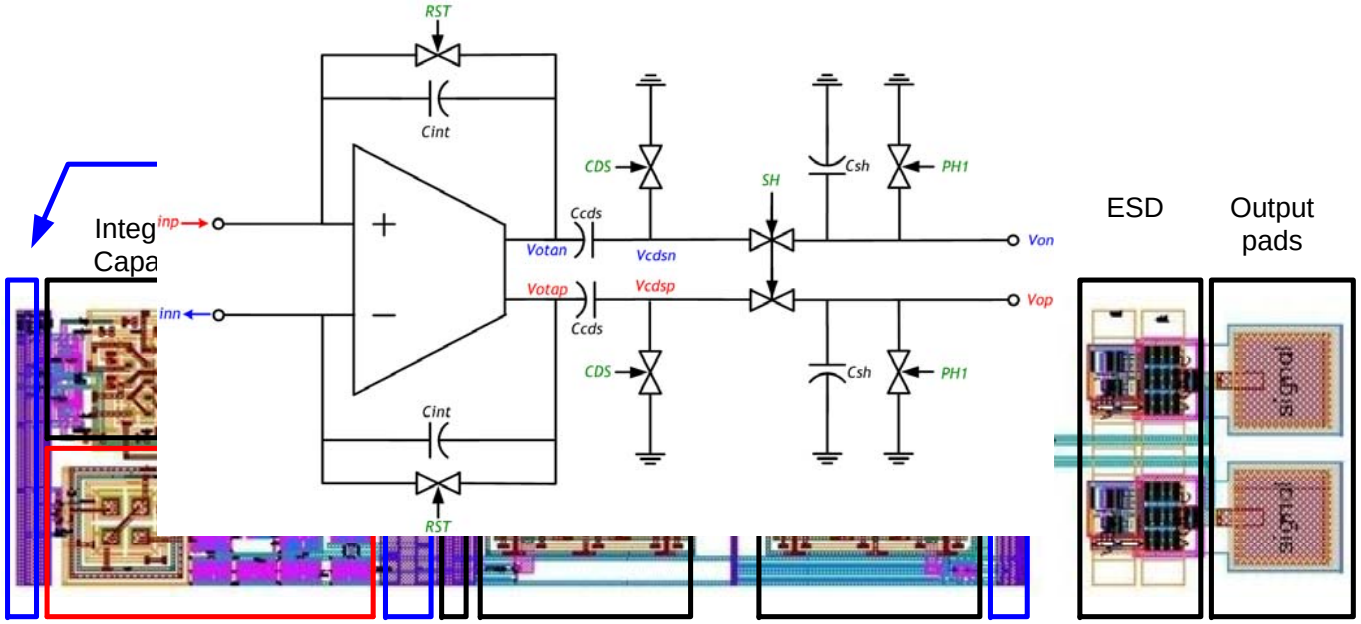
Size

1500 *μm length*

400 μm height

Four times the height of the detector element

Increases scalability

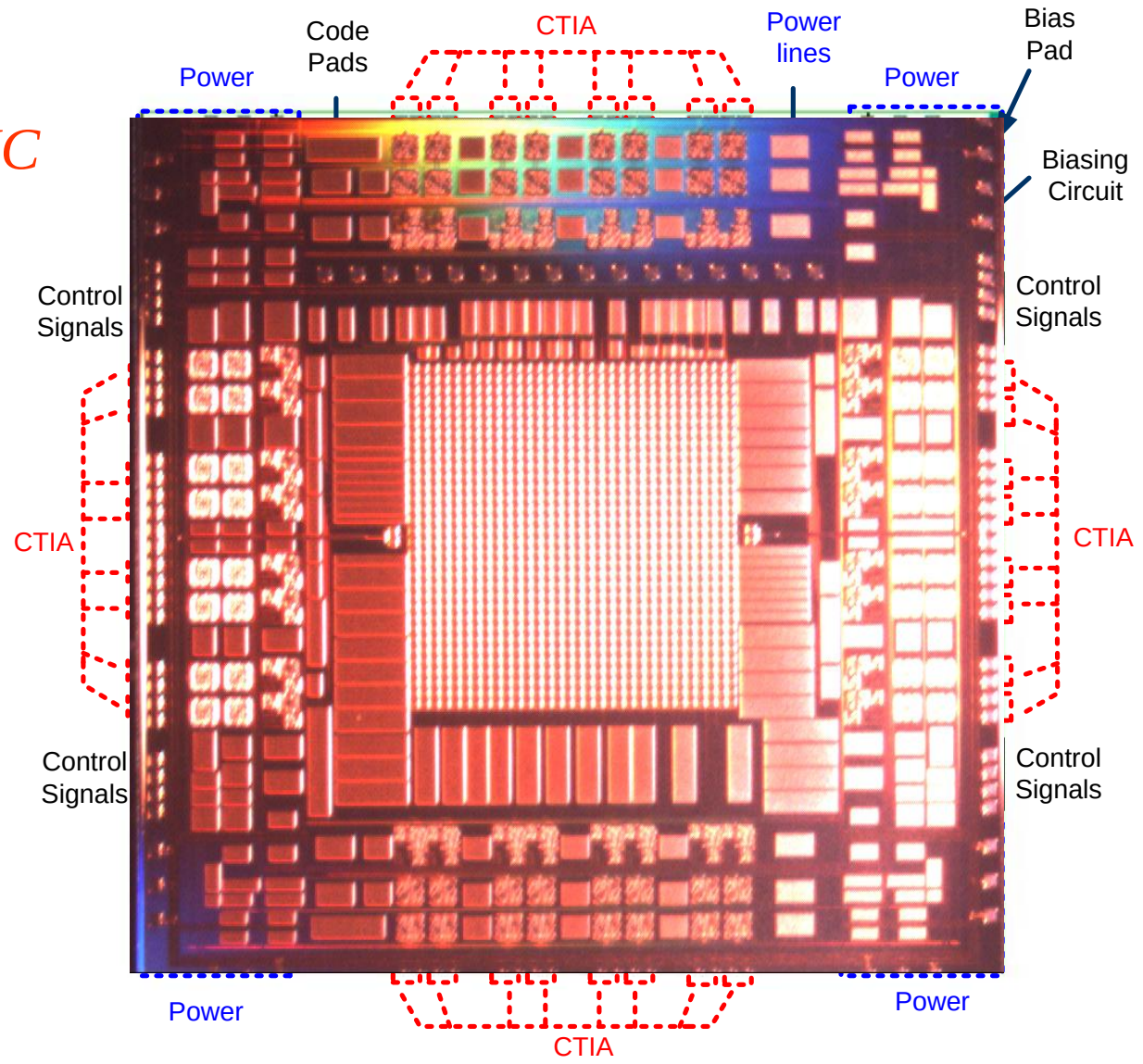


Design Implementation

Full IC Layout

Fabricated Test ROIC

- *8.4 x 8.4 mm²*
- *Symmetric*
- *Scalable*
  - *A 64x32 System*



Design Implementation

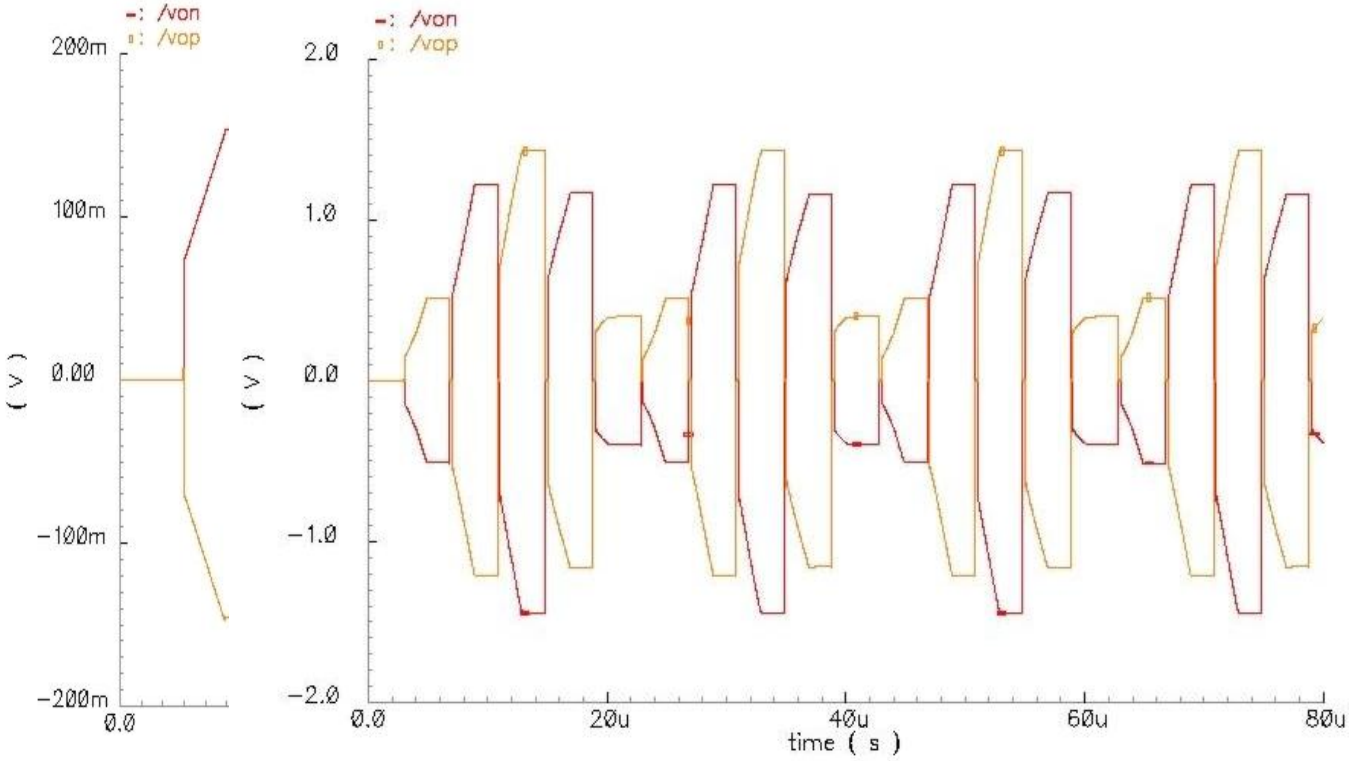
Post-layout Simulations

DC INPUT CURRENT

25kHz, 50nA pk INPUT CURRENT ENCODED @ 1MHz

NON ENCODED

i_{in} = 5nA, i_{ip} = - 5nA



Sinusoidal Characteristic

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Future Work

Testing Methodology